

REMARKS

Claims 1 - 20 were pending in the present application for patent as of the Office Action of March 28, 2003. In the Office Action of March 28, 2003, the Examiner objected to claims 1, 9, 14, and 18, rejected claims 4, 12, and 20 under 35 U.S.C. 112, second paragraph, rejected claims 1 - 3, 9 - 11, 13 - 15, and 17 - 19 under 35 USC 102(e) as being anticipated by U.S. Patent Number 6,476, 580, Nakamiya et al., and rejected claims 4 - 8, 12, 16, and 20 under 35 USC 103(a) as being unpatentable over Nakamiya et al. as applied to claim 3, in view of U.S. Patent Number 4,491,424, Ito et al.

By this amendment, the applicants have amended claims 1, 4, 9, 12, 14, 19, and 20.

Claims 1, 9, 14, and 18 were objected to because they had a semi-colon after the word "comprising". In response, claims 1, 9, 14, and 18 have been amended to substitute a colon for the semi-colon.

Claims 4, 12, and 20 were rejected under 35 U.S.C. 112, second paragraph, because of the use of the word "substantially". In response, claims 4, 12, and 20 have been amended in a manner believed to overcome the examiner's section 112 based rejection.

Claims 1 - 3, 9 - 11, 13 - 15, and 17 - 19 were rejected under 35 USC 102(e) as being anticipated by Nakamiya et al. The applicants believe that claims 1 - 3, 9 - 11, 13 - 15, and 17 - 19, as originally filed, are not anticipated by Nakamiya et al. Generally, Nakamiya et al. discloses a timepiece apparatus having a generator for generating AC power, an AC magnetic-field detecting circuit, a storage device for storing the generated power, and a stepping motor. The AC magnetic-field detection circuit detects generator output and provides signals that are used for controlling motor-driving pulses. FIG. 7 of Nakamiya et al. discloses a generation detecting circuit. The generation detecting circuit includes two comparators (COMP1 and COMP2) for detecting generation output (see column 24, line 6 to column 25, line 39). The outputs of the comparators are provided to a NAND gate 201. The output of the NAND gate is provided to a smoothing circuit 202. The smoothing circuit includes a R-C integrating circuit and is used to remove switching noise causing by operation of the NAND gate.

Nakamiya et al. does not show or suggest an apparatus for detecting a stall condition of a stepping motor as claimed in any of the originally filed claims of the present application. For example, Nakamiya et al. does not disclose that the stepping motor is of the type that includes

at least first and second coils as claimed in claim 1. In Nakamiya et al. the stepping motor 10 only has one driving coil 11. Also, Nakamiya et al. does not disclose an integrator as claimed in claim 1, where the integrator receives signals from a current generator used to provide drive currents to the first and second coils, and where the signals result from motion of the rotor. In Nakamiya et al., the integrator (smoothing circuit 202) is part of the generation detecting circuit for detecting if power is being generated by the AC generator. The integrator of Nakamiya et al. is not used as part of a circuit to detect rotor motion of a stepping motor as claimed in claim 1. In addition, Nakamiya et al. does not disclose a comparator coupled to the integrator for comparing an integrated version with a predetermined threshold to detect the stall condition as claimed in claim 1. In Nakamiya et al. the comparators detect generation output. The output of the comparators is provided to a NAND gate and then to an integrator. Further, the apparatus of Nakamiya et al. is not even used to detect a stall condition of a stepping motor. In other words, Nakamiya et al. does not show or suggest a single element of claim 1. Therefore, the applicants believe that claim 1, as originally filed, is allowable over Nakamiya et al.

The applicants believe that the comments above regarding the rejection of claim 1 also applies to the rejection of claims 2 - 3, 9 - 11, 13 - 15, and 17 - 19, and that claims 2 - 3, 9 - 11, 13 - 15, and 17 - 19 are allowable over Nakamiya et al.

Claims 4, 12, 16 and 20 were rejected under 35 USC 103(a) as being unpatentable over Nakamiya et al. as applied to claim 3 in view of Ito et al. The applicants believe that the comments above regarding the rejection of claim 1 also applies to the section 103 based rejection of claims 4, 12, 16 and 20, and that claims 4, 12, 16 and 20 are allowable over Nakamiya et al. as applied to claim 3 in view of Ito et al.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Believing to have responded to each and every rejection contained in the Office Action mailed March 28, 2003, Applicants respectfully request the reconsideration and allowance of claims 1 - 20; thereby placing the application in condition for allowance.

Respectfully submitted,

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MESSAGE:

Enclosed herewith, please find a FORMAL AMENDMENT for filing in the below-identified application. If Applicant has overlooked any fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit 502117.

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:

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PLEASE GIVE THESE PAPERS TO:

EXAMINER: Renata D. McCloud
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